Application No. 10/099,707
Amendment dated September 17, 2003
Reply to Office Action of March 17, 2003

Amendments to the Specification:

Please replace the paragraph that begins at page 7, line 22 and ends at page 8, line 5 with the following amended version of that paragraph:

Each transistor (other than the default transistor) in each group of parallel transistors is activated/deactivated via a multiplexer that is controlled by other associated circuitry. For example, RL1b and RL2b are controlled in tandem by the output signal of multiplexer 110b. This multiplexer is controllable to output either VDD (which turns off transistors RL1b and RL2b) or RCONT (which gives RL1b and RL2b exactly the same control as RL1a and RL2a). [[the]] The latter condition of multiplexer 110b causes RL1a and RL1b to operate in parallel with one another, and similarly causes RL2a and RL2b to operate in parallel with one another. Other multiplexers in the group 110b-110n operate similarly to allow other transistors in the groups RL1b-RL1n and RL2b-RL2n to be selectively added into parallel operation with default transistors RL1a and RL2a.

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Please replace the paragraph that begins at page 9, line 22 and ends at page 10, line 10 with the following amended version of that paragraph:

Returning to FIG. 4, all ranges of operation of illustrative programmable differential delay cell 40' (i.e., ranges a-n) have the same operating limits on RCONT and VCONT as the traditional delay cell. Nevertheless, much higher ~~frequency~~ frequencies can be achieved by turning on optional devices (ranges b-n). This is due to the reduced load resistance, which reduces delay cell time [constant] as described previously. Extra transistors in

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the current mirror provide more total tail current IBIAS, which maintains the output swing, while extra load transistors add more resistors in parallel to reduce the load resistance. In the programmable delay cell the load resistance RL becomes a parallel combination of multiple load resistors according to the equation 1/RL = 1/RLa + 1/RLb + ... + 1/RLn. When all resistors are equal with a value of R, then the total resistance is simply R/n, which shows that the load resistance will decrease as more optional transistors are activated. If all resistors are not equal, then the total resistance of an arbitrary number of resistors in parallel is always less than the smallest resistor in the combination.

Please replace the paragraph that begins at page 13, line 15 and ends at page 14, line 4 with the following amended version of that paragraph:

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It will be understood that the foregoing is only illustrative of the principles of the invention, and that various modifications can be made by those skilled in the art without departing from the scope and spirit of the invention. For example, although FIG. 4 at least pictorially implies that the sources of the control signals for PLCs [[100]] 110, on the one hand, and PLCs 120, on the other hand, are separate, common or shared control may be used if desired. Such common or shared control would typically mean that the same control would be used for PLCs 110b and 120b, that the same control would be used for PLCs 110c and 120c, etc. As another example of modifications within the scope of the invention, any number of parallel transistors can be included in each group RL1a-n, RL2a-n, and ICONTa-n. Although differential delay cells are

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generally preferred, the invention can also be applied to non-differential delay cells. For example, such a non-differential delay cell would have only one switching transistor SW1 or SW2, and only one set of load resistor transistors RL1a-n or RL2a-n. In other respects, such a non-differential delay cell can be constructed as shown, for example, in FIG. 4.